WHAT IS CLAIMED IS:

1. A method for forming a thin film field effect transistor comprising:

forming a preliminary substrate having at least a silicon layer, a first dielectric layer, and a gate metal layer stacking up sequentially;

forming a photoresist layer on top of the preliminary substrate;

selectively removing a portion of the photoresist layer in a single exposure process to form a first photoresist pattern having a two-portion structure with a first portion having a first width and a second portion underneath the first portion with a second width;

removing the gate metal layer, the first dielectric layer, and the silicon layer to have the same width as the second width;

selectively reducing the first photoresist pattern to form a second photoresist pattern having the first width;

reducing the gate metal layer to have the same width as the first width using the second photoresist pattern; and

doping a predetermined impurity in the silicon layer for forming a source region and a drain region of a predetermined type in areas not directly underneath the reduced gate metal layer.

2. The method of claim 1 further comprising forming a second dielectric layer for covering the gate metal layer and exposing the source and drain regions by having openings through the first dielectric layer; and

forming a first conducting layer making connection with the source and drain regions through the openings.

3. The method of claim 2 further comprising forming a passivation layer on top of the first conducting layer and the second dielectric layer.

4. The method of claim 3 wherein the forming a passivation layer further includes:

forming one or more connection openings for connecting the first conducting layer to a second conducting layer; and

forming the second conducting layer to make connections to the first conducting layer.

5. The method of claim 1 wherein the selectively removing a portion of the photoresist layer further includes selectively exposing the photoresist layer to a light source by using a predetermined mask with a first and second regions, the first region passing less light than the second region for forming the two-

portion structure.

6. The method of claim 5 wherein the first and second regions of the mask are made of different materials.

7. A method for forming a thin film field effect transistor comprising:

forming a preliminary substrate having at least a silicon layer, a first dielectric layer, and a gate metal layer stacking up sequentially;

forming a photoresist layer on top of the preliminary substrate;

selectively removing a portion of the photoresist layer using a predetermined mask in a single exposure process to form a first photoresist pattern having a two-portion structure with a first portion having a first geometry and a second portion underneath the first portion with a second geometry;

trimming the gate metal layer, the first dielectric layer, and the silicon layer to have the second geometry;

selectively reducing the first photoresist pattern to form a second photoresist pattern having the first geometry;

reducing the gate metal layer to have the same geometry as the first geometry using the second photoresist pattern; and

doping a predetermined impurity in the silicon layer for forming a source

region and a drain region of a predetermined type in areas not directly underneath the reduced gate metal layer.

8. The method of claim 7 further comprising forming a second dielectric layer for covering the gate metal layer and exposing the source and drain regions by having openings through the gate oxide layer; and

forming a conducting layer to reach the source and drain regions through the openings.

9. The method of claim 8 further comprising forming a passivation layer on top of the conducting layer and the second dielectric layer.

10. The method of claim 9 wherein the forming a passivation layer further includes forming one or more connection openings for connecting the conducting layer to a routing metal layer formed on top of the passivation layer.

11. The method of claim 7 wherein the predetermined mask has a center and surrounding regions, the center region passing less light than the surrounding region for forming the two-portion structure.

12. The method of claim 11 wherein the center and surrounding regions of the mask are made of different materials with the material for the center region shielding more light than the material for the surrounding region.

13. The method of claim 11 wherein the first and second regions of the mask are made from a same material with a predetermined mask pattern on the surrounding region for hindering the light from passing therethrough.

14. A method for forming a thin film field effect transistor on a substrate, the substrate having at least a silicon layer, a first dielectric layer, and a gate metal layer stacking up sequentially, the method comprising:

forming a photoresist layer on top of the substrate;

forming a first photoresist pattern in a single exposure process, the first photoresist pattern having a step structure with a center portion having a first width narrower than a second width of a bottom portion underneath;

trimming the gate metal layer, the first dielectric layer, and the silicon layer to have the same width as the second width;

reducing the first photoresist pattern to form a second photoresist pattern having the first width;

reducing the gate metal layer to have the same width as the first width

using the second photoresist pattern;

doping a predetermined impurity in the silicon layer for forming a source region and a drain region of a predetermined type in areas not directly underneath the reduced gate metal layer;

forming a second dielectric layer for covering the gate metal layer and exposing the source and drain regions by having openings through the gate oxide layer; and

forming a first conducting layer to reach the source and drain regions through the openings; and

forming a passivation layer on top of the conducting layer and the second dielectric layer with one or more connection openings for connecting the first conducting layer to a second conducting layer.

15. The method of claim 14 wherein the routing layer is an indium tin oxide layer.

16. The method of claim 14 wherein forming a first photoresist pattern further includes using a predetermined mask having a first and second regions, the first region passing less light than the second region for forming the step structure.

17. The method of claim 16 wherein the first and second regions of the mask are made of different materials with the material for the first region shielding more light than the material for the second region.

18. The method of claim 16 wherein the first and second regions of the mask are made from a same material with a predetermined mask pattern covering the second region for hindering the light from passing therethrough.

19. The method of claim 14 wherein the reducing the first photoresist pattern further includes using a dry etch process to reduce the first photoresist pattern.

20. The method of claim 14 wherein the reducing the first photoresist pattern further includes using an auto plasma process to reduce the first photoresist pattern.